ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

تلخيص لمادة:

مختبر منطق والكترونيات

جزيل الشكر للطالب:

حمزة اسماعيل

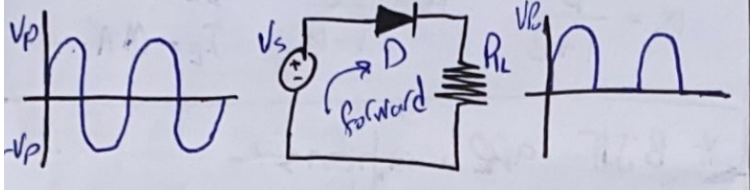
*Logic and Electronic laboratory :-

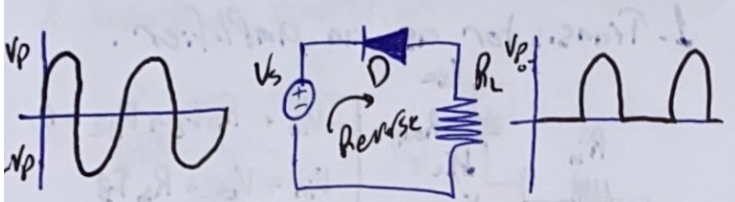
*Diode Applications :-

*Regular Diode Applications :-

1- The Rectifier Circuits :-

A- Half Wave rectifier (HWR) :-





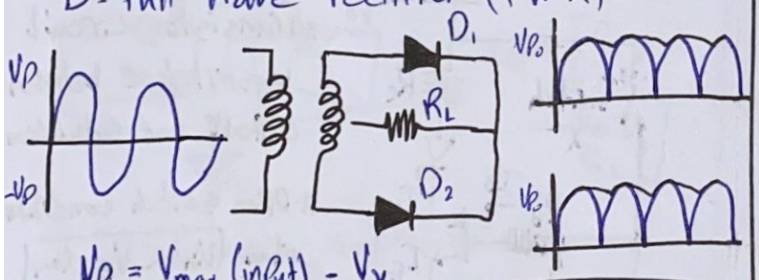
$V_{p_o} = V_{max}(input) - V_\gamma$ $\quad$ $V_\gamma = 0.7V$

$V_{avg} = \frac{V_p}{\pi} = 0.318\ V_p$.

$f_o = f_{source}$.

$$V_r = \frac{V_p}{f_{source} \cdot R.C}$$

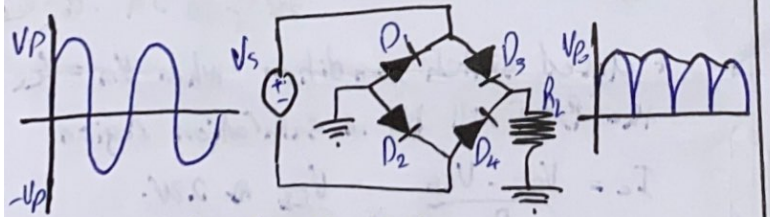
B- Full wave rectifier (FWR) :-



$V_{p_o} = V_{max}(input) - V_\gamma$

$f_o = 2\, f_{source}$

$$V_r = \frac{V_p}{2 f_{source} R.C}$$



$V_{p_o} = V_{max}(input) - 2V_\gamma$.

$V_{avg} = \frac{2V_p}{\pi} = 0.636\ V_p$.

$f_o = 2\, f_{source}$.

$V_{DC} = V_{p_o} - \frac{1}{2} V_r$

max Voltage input signal

$$V_r = \frac{V_p}{2 f_{source} RC}$$

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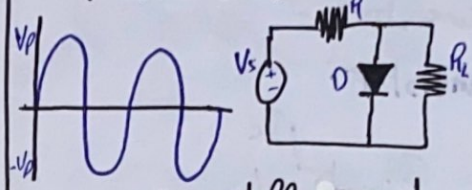
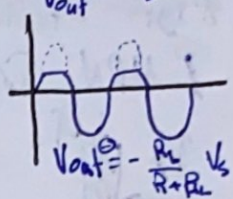
*Regular Diode Applications :-

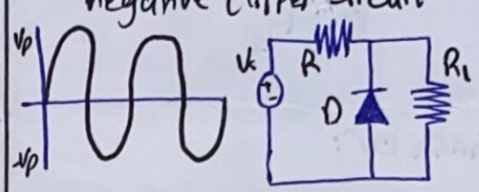
2- Clipper Circuits → Cutting.

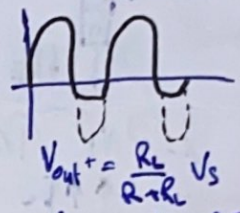
Positive clipper circuit



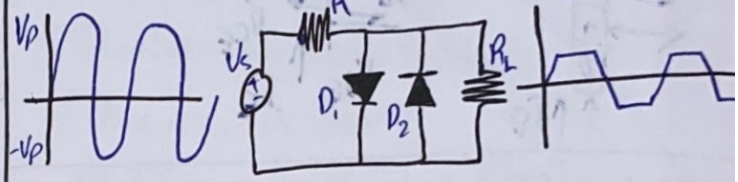


negative clipper circuit





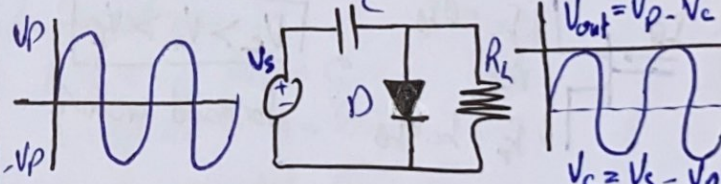
dual clipper circuit.



3- clamper circuits :- → shifting.

Positive clamper

negative clamper.



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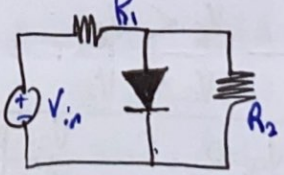
*clipper :- cutting



Positive

$V_{max} = V_D = 0.7$

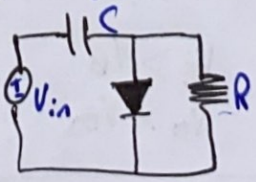
$V_{min} = \frac{-R_2}{R_1 + R_2} V_{in}$

negative

$V_{max} = \frac{R_2}{R_1 + R_2} V_{in}$

$V_{min} = -V_D = -0.7$

*clamper :- shifting.



$2\pi RC \gg 5\ T$.

$2\pi RC \gg 5\ \frac{1}{f}$.

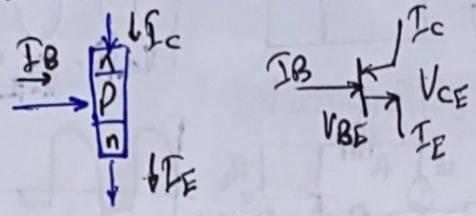
$C \gg \frac{5}{2\pi f R}$

* Logic and Electronics Laboratory :-

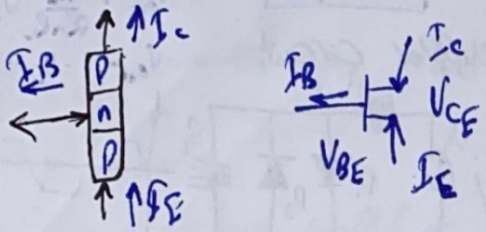
* Bipolar Junction Transistor (BJT) :-

* Type of Transistor :-

1. NPN Transistor.

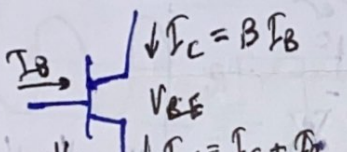


2. PNP Transistor:



* Mode of operation for the Transistor.

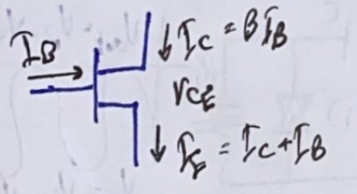
1. Reverse Active mode.



$V_C < V_B < V_E$

active → Rev

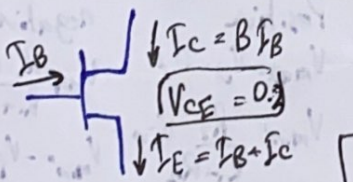
2. forward Active mode.



$V_C > V_B > V_E$

forward active

3. Saturation mode :

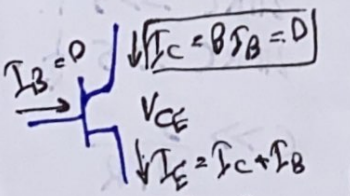


$V_E < V_B$

$V_C < V_B$

$V_{CE} = 0$, $I_C = \frac{V_{cc} - 0.2}{R_c}$

4. Cutt off mode.



$V_E > V_B$

$V_C > V_B$

$I_C = 0$, $V_{CE} = V_{cc}$

* Current Relationship :-

$I_E = I_C + I_B \Rightarrow I_E = I_B (1 + B)$.

$I_C = B I_B$

$\frac{I_C}{I_E} = \alpha$, $I_C = \alpha I_E$.

$\alpha = \frac{B}{1+B}$, $B = \frac{\alpha}{1-\alpha}$

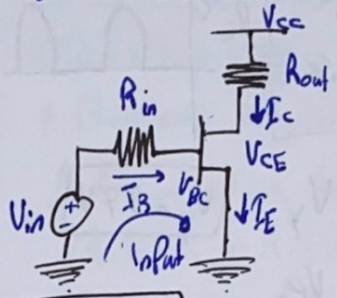
I_B = μA

I_C = mA

I_E = mA.

* BJT applications :-

1. Transistor as an amplifier.



$-V_{in} + R_{in} I_B + V_{BC} = 0$.

$V_{in} = V_{BC} + R_{in} I_B$.

$I_C = B I_B$.

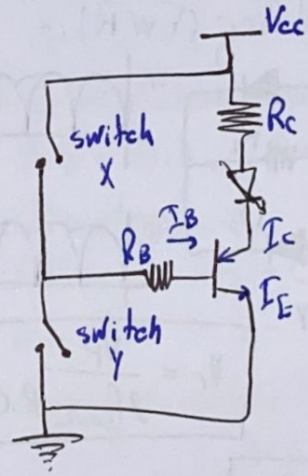
$I_E = I_C + I_B$.

BE → Fw
BC → Rev
amplifier

$-V_{cc} + R_{out} I_C + V_{CE} = 0$.

$V_{cc} = V_{CE} + R_{out} I_C$.

2. Transistor as switch :-



* Transistor circuit is switched between Cutoff and saturation

* Open switch condition when $V_{in} < V_{BE(on)}$ the BJT will be in Cutt off region

$I_B = I_C = 0$ A. $V_o = V_{cc}$

* closed switch condition when $V_{in} = V_{cc}$ the BJT will be in saturation region

$I_c = \frac{V_{cc} - V_{CE}}{R_c}$ $V_{CE} \approx 0.2$V.

BE → Fw , BC → Fw
BE → Rev , BC → Rev
switching.

* Logic and Electronics laboratory :-

* Operational amplifier :-

* Ideal op-amp :

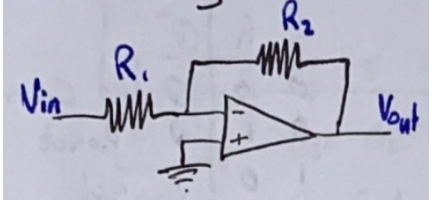
1- Infinite input resistance

2- Zero output resistance.

3- Zero input Current and input Voltage offsets.

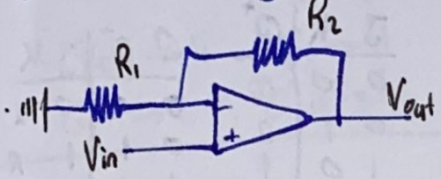
* Types of op-amp :-

1 Inverting amplifier.



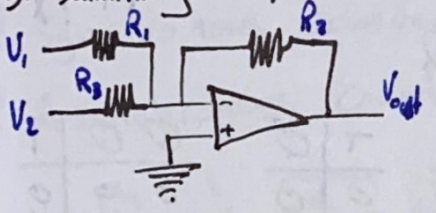
$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

2. Non-Inverting amplifier



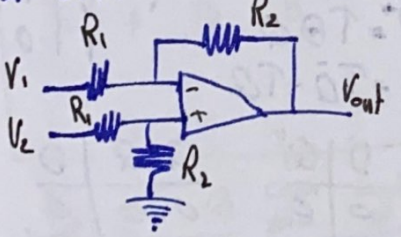
$$V_{out} = \frac{R_2}{R_1} V_{in}.$$

3- Summing amplifier



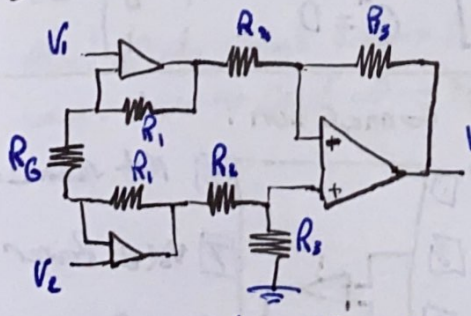
$$V_{out} = -\left[\frac{R_2}{R_1} V_1 + \frac{R_2}{R_3} V_2\right].$$

4- Difference amplifier :-



$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1)$$

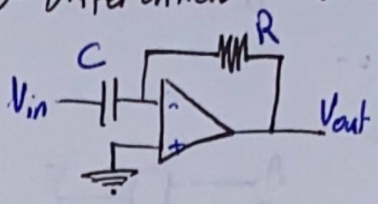
5- Instrumentation amplifier :-



$$V_{out} = \left(1 + \frac{2R_1}{R_G}\right)\left(\frac{R_3}{R_2}\right)(V_2 - V_1)$$

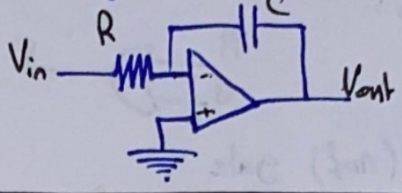
* Types of op-amp :-

6- Differential amplifier :-



$$V_{out} = -RC\frac{dV_{in}}{dt}$$

7- Integration amplifier :-



$$V_{out} = \frac{-1}{RC}\int V_{in} dt$$

* Combinational logic :-

* Boolean algebra Theorems :-

1- Associative law :-

$(A.B).C = A.(B.C) = ABC.$

$(A+B)+C = A+(B+C) = A+B+C$

2- Distributive law :-

$A.(B+C) = AB+AC.$

$A+(B.C) = (A+B)(A+C).$

3- Commutative law :-

$A.B = B.A. \quad A+B = B+A.$

4- Precedence :-

$A.B + C = AB + C.$

$A + (B.C) = A + BC.$

5- Single Variable Theorems :-

$AA = A \quad . \quad A+A = A.$

$A+\bar{A} = 1 \quad . \quad A\bar{A} = 0 \quad . \quad \bar{\bar{A}} = A$

$A + AB = A \quad . \quad A + \bar{A}B = A+B$

$A.1 = A \quad . \quad A+1 = 1 \quad . \quad A+0 = A$

$A.0 = 0 \quad \bar{1} = 0 \quad . \quad \bar{0} = 1$

6- Demorgan's Theorems :-

$\overline{(A.B)} = \bar{A} + \bar{B}$

$\overline{(A+B)} = \bar{A}.\bar{B}$

7- Absorption Theorems :-

$A + AB = A \quad . \quad A(A+B) = A$

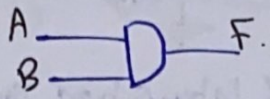
* Logic and Electronics Laboratory :-

* Combinational logic :-

* Logic gates :-

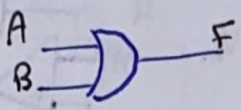
1. AND gates :-

$A \cdot B = F$



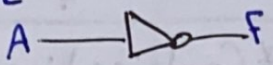
2. OR gates :-

$A + B = F$



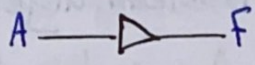
3. Inverter (not) gate

$F = \bar{A}$



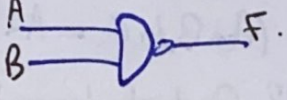
4. Buffer gates :-

$F = A$



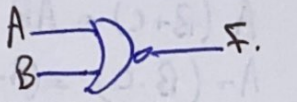
5. NAND gates.

$F = \overline{A \cdot B} = \bar{A} + \bar{B}$



6. NOR gates :-

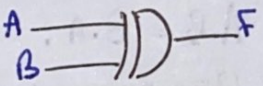
$F = \overline{(A+B)} = \bar{A}\bar{B}$



7. Exclusive OR (XOR) :-

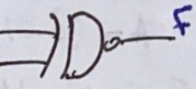
$F = A \oplus B$

$= \bar{A}B + A\bar{B}$



8. Exclusive NOR (XNOR)

$F = \overline{A \oplus B} = \overline{\bar{A}B + A\bar{B}} = \bar{A}\bar{B} + AB$

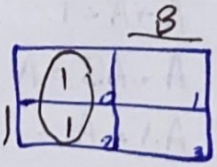


* Karnagh map (K-map) :-

1. Two Variable.

$F(A,B) = \Sigma(0,2)$

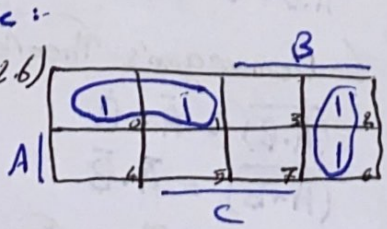
$F(A,B) = \bar{B}$.



2. Three Variable :-

$F(A,B,C) = \Sigma(0,1,2,6)$

$F(A,B,C) = \bar{A}\bar{B} + B\bar{C}$

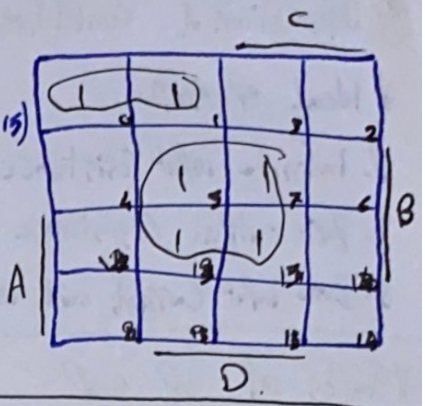


* Karnagh map (K-map) :-

3. four Variable

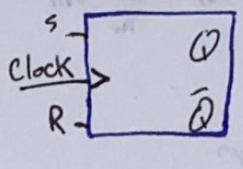
$f(A,B,C,D) = \Sigma(0,1,5,7,13,15)$

$F(A,B,C,D) = \bar{A}\bar{B}\bar{C} + BD$



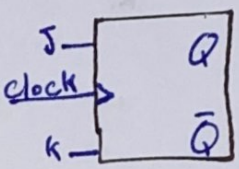
* Sequential logic :-

1. SR flf



S	R	Q^+	
0	0	Q	no change
0	1	0	Reset
1	0	1	Set.
1	1	X	invalid

2. JK flf :-

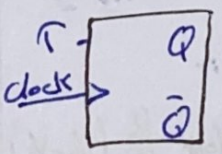


J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Q^+ = J\bar{Q} + \bar{K}Q$

3. T flf :



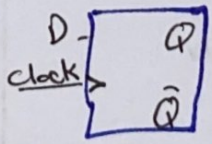
T	Q^+
0	Q
1	$\bar{Q}$

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q^+ = T \oplus Q$

$= T\bar{Q} + \bar{T}Q$

4. D flf

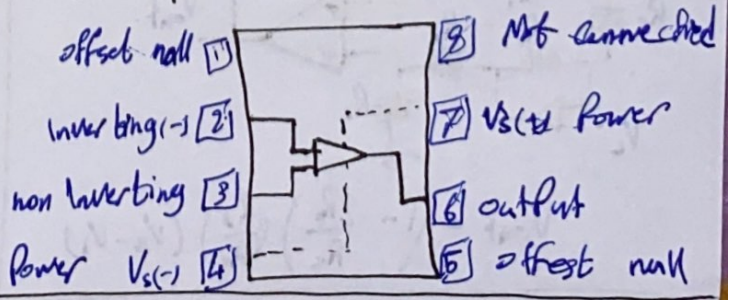


D	Q^+
0	0
1	1

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

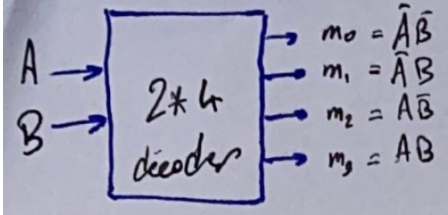
$Q^+ = D$

* OP amp connection.

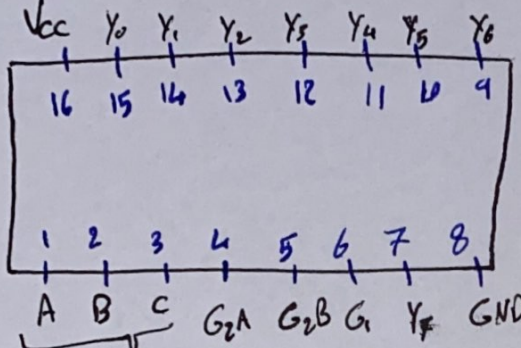


* Logic and Electronic laboritory :-

* Decoder :-



$n=2 \rightarrow$ Output $= 4$
$n=3 \rightarrow$ Output $= 8$
$n=4 \rightarrow$ Output $= 16$



$G_2 = G_2A + G_2B$.

$L = L + L$.

$V_{cc} \rightarrow H$, $G_1 \rightarrow H$.

$G_2A \rightarrow L$, $G_2B \rightarrow L$. , GND $\rightarrow L$.

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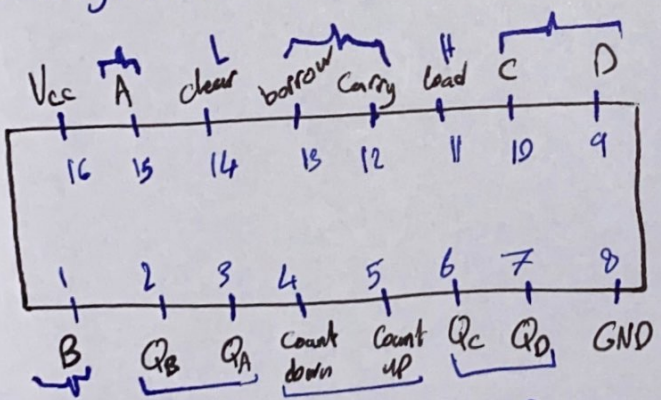
* Counter :-

1. Synchronous counters.
2. Asynchronous counters.



DCBA $\rightarrow$ D - MSB , A $\rightarrow$ LSB.

Count up $\Rightarrow$ Count down $\rightarrow H$.

Count down $\Rightarrow$ Count up $\rightarrow H$.